Refine Search

Your wildcard search against 10000 terms has yielded the results below.
Your result set for the last L# is incomplete.
The probable cause is use of unlimited truncation. Revise your search strategy to use limited truncation.
Search Results -

Terms	Documents
L22 same correspond$	1

Database: US Pre-Grant Publication Full-Text Database; US Patents Full-Text Database; US OCR Full-Text Database; EPO Abstracts Database; JPO Abstracts Database; Derwent World Patents Index; IBM Technical Disclosure Bulletins

Search: L24

Refine Search | Recall Text | Clear | Interrupt

Search History

DATE: Friday, January 21, 2005 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
DB=USPT,USOC,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR			
L24	L22 same correspond$	1	L24
L23	L22 same relevant	0	L23
L22	L1 same storage	31	L22
L21	L20 same memory	2	L21
L20	plurality same l1	18	L20
L19	plurality adj2 l1	0	L19
L18	L17 and l16	0	L18
L17	earlier adj2 repair	39	L17
L16	preparing near3 repair	208	L16
L15	L14 and l1	0	L15
L14	redundancy adj1 register	76	L14
L13	L10 same redundant	17	L13

L12	L11 and l10	1	L12
L11	bisr	346	L11
L10	L9 same l7	618	L10
L9	row adj1 address	19730	L9
L8	L7 and l1	0	L8
L7	L6 near3 register	1116	L7
L6	column adj1 address	19769	L6
L5	coulumn adj1 address	0	L5
L4	L3 and l1	31	L4
L3	redundant same memory same array	4535	L3
L2	L1 same register	6	L2
L1	redundant adj3 plane	155	L1

END OF SEARCH HISTORY

First Hit Fwd Refs Previous Doc Next Doc Go to Doc#
Generate Collection Print

L21: Entry 1 of 2 File: USPT Aug 24, 2004

DOCUMENT-IDENTIFIER: US 6781896 B2
TITLE: MRAM semiconductor memory configuration with redundant cell arrays

Brief Summary Text (14):
With the foregoing and other objects in view there is provided, in accordance with the invention, an MRAM semiconductor memory configuration, comprising: a memory matrix of a plurality of MRAM main cell arrays arranged in a crosspoint array or a transistor array and a plurality of redundant MRAM cell arrays formed with redundant MRAM memory cells, the plurality of MRAM main cell arrays together with the plurality of redundant MRAM cell arrays being disposed in a plurality of planes commonly integrated in a given chip; and wherein the redundant MRAM cell arrays are distributed over individual the planes of the memory matrix such that defective memory cells in one plane can be replaced with redundant memory cells from other planes.

Previous Doc Next Doc Go to Doc#

US006781896B2

(12) **United States Patent**
Lammers et al.

(10) **Patent No.: US 6,781,896 B2**
(45) **Date of Patent: Aug. 24, 2004**

(54) **MRAM SEMICONDUCTOR MEMORY CONFIGURATION WITH REDUNDANT CELL ARRAYS**

(75) Inventors: **Stefan Lammers**, South Burlington, VT (US); **Dietmar Gogl**, Essex Junction, VT (US); **Gerhard Müller**, Meitingen (DE)

(73) Assignee: **Infineon Technologies AG**, Munich (DE)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 69 days.

(21) Appl. No.: **10/135,416**

(22) Filed: **Apr. 30, 2002**

(65) **Prior Publication Data**

US 2002/0159317 A1 Oct. 31, 2002

(30) **Foreign Application Priority Data**

Apr. 30, 2001 (DE) 101 21 182

(51) **Int. Cl.**[7] **G11C 7/00**

(52) **U.S. Cl.** **365/200**; 365/158; 365/230.03

(58) **Field of Search** 365/200, 158, 365/230.03

(56) **References Cited**

U.S. PATENT DOCUMENTS

5,257,229	A *	10/1993	McClure et al.	365/200
5,359,560	A *	10/1994	Suh et al.	365/200
5,381,370	A *	1/1995	Lacey et al.	365/200
6,154,413	A	11/2000	Longwell et al.	
6,351,408	B1 *	2/2002	Schwarzl et al.	365/158
6,400,602	B2 *	6/2002	Takata et al.	365/185.09

FOREIGN PATENT DOCUMENTS

DE 197 44 095 A1 4/1999

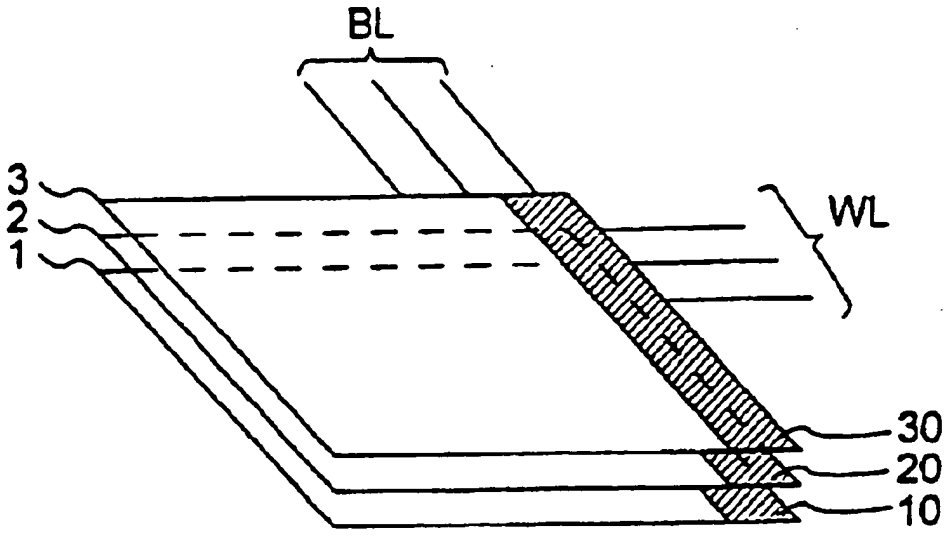
* cited by examiner

Primary Examiner—Hoai Ho
(74) *Attorney, Agent, or Firm*—Laurence A. Greenberg; Werner H. Stemer; Ralph E. Locher

(57) **ABSTRACT**

The MRAM semiconductor memory configuration has MRAM main cell arrays in the form of a crosspoint array or a transistor array together with redundant MRAM cell arrays formed of redundant MRAM memory cells arranged in a plurality of planes and provided on the same chip. The redundant MRAM cell arrays are distributed over the individual planes of the memory matrix or one plane of the memory array is used in its entirety for providing redundant cell arrays.

16 Claims, 2 Drawing Sheets



L12: Entry 1 of 1 File: USPT Oct 16, 2001

DOCUMENT-IDENTIFIER: US 6304989 B1
TITLE: Built-in spare row and column replacement analysis system for embedded memories

Abstract Text (1):
A built-in replacement analysis (BIRA) circuit allocates spare rows and columns of cells for replacing rows and columns of an array of memory cells in response to an input sequence of cell addresses, each identifying a row address and a column address of each defective cell of the cell array. The BIRA subsystem, including a row register corresponding each spare row and a column register corresponding to each spare column, responds to incoming cell addresses by writing their included row address into the row registers, by writing their column addresses into the column registers, and by writing link bits into the column registers. Each link bit links a row and a column register by storing row and column addresses of a defective cell. The BIRA subsystem also writes a "multiple cell" bit into each row register to indicate when the row address it stores includes more than one defective cell. The row and column addresses stored in these registers indicate the array rows and columns for which spare rows and columns are to be allocated. Each row and column register also includes a "permanent" bit the BIRA subsystem sets to indicate when the spare row or column allocation indicated by its stored row or column address is permanent. The BIRA subsystem efficiently allocates spare row and columns by manipulating the data stored in the row and column registers in response to a sequence of defective cell address.

Brief Summary Text (3):
The present invention relates in general to built-in self-repair (BISR) systems for integrated circuits employing embedded memories, and in particular to a BISR system employing an efficient spare row and column replacement analysis system.

Brief Summary Text (10):
For many reasons it is desirable to provide an ASIC with a "built-in self-repair" (BISR) system that can test and repair a memory with little or no communication with devices external to the ASIC. For example radiation or other environmental factors can cause a memory cell in an ASIC to fail long after it has passed a test at the factory. When the ASIC includes a BISR system enabled, for example, on ASIC power up or in response to an externally generated enabling signal, the BISR system can automatically test for and replace damaged cells. Since the BISR system is wholly contained within the ASIC, it isn't necessary to remove the ASIC from its normal operating environment or to connect it to external test and repair equipment.

Brief Summary Text (11):
Self-contained BISR systems have not been able to take full advantage of the efficiencies provided by combined spare column and spare row replacement because it has not been practical for them to store test results for all cells so that they can be analyzed at the end of the test to determine the best way to allocate spare rows and columns. U.S. Pat. No. 5,764,878 issued Jun. 9, 1998 to Kablanian et al describes a BISR system that organizes memory columns into blocks of several

columns each and tests and repairs each block in turn. If a block of columns has one or more defective cells, a built-in repair analysis (BIRA) subsystem of the BISR system decides whether to repair the block by replacing memory rows with spare rows or by replacing the entire block with a spare block. Since the BISR system only tests and repairs one memory block at a time, it doesn't have to store and analyze test results data for the entire memory array at once. However since the BIRA subsystem makes its row and column replacement selections without having fully mapped the defective cells of the memory, the BISR System will not always optimize its allocation of spare rows and column blocks. Since the described BIRA system tests first on a row-by-row basis and then on a column-by-column basis, the system may impact test flexibility insofar as blocks must be tested individually and will have an effect on test time.

Brief Summary Text (12):
U.S. Pat. No. 5,577,050 also describes a BISR system employing both spare row and spare column replacement. The BISR system first checks each column in turn to determine whether the column has a "global" fault (such as column line stuck or open faults) that can affect more than one cell of a column. However it does not individually test each cell of a column. When it finds such a global error in a column, the BISR system replaces the defective column with a spare column before moving on to test the next column. After it has tested and replaced defective columns, the BISR system then individually tests each memory cell on a row-by-row basis, replacing any row having a defective cell with a spare row. Since it tests and repairs on a column-by-column and row-by-row basis, the BISR system doesn't have to store a large amount of result data, but the system will not optimize spare row and column allocation for, example, when a column has two or more defective cells that are not due to a global column fault.

Brief Summary Text (13):
What is needed is a BIRA subsystem for a BISR system for substantially optimizing spare row and column replacement allocation based on system test results without having to concurrently store large amounts of test results data upon which to base its allocation decisions and which does not limit test flexibility or significantly increase test time.

Brief Summary Text (15):
A built-in self-repair (BISR) system for testing and reconfiguring an array of rows and columns memory cells embedded in an integrated circuit includes a built-in replacement analysis (BIRA) subsystem for allocating spare rows and columns of memory cells for replacing array rows and columns containing defective memory cells. The BIRA subsystem allocates spare rows and columns of cells for replacing rows and columns of an array of memory cells in response to an input sequence of cell addresses generated by a built-in self-test (BIST) subsystem, a portion of the BISR system. The BIST subsystem tests the memory array and generates a cell address for each defective cell in the array, the cell address including the row address and a column address of the defective cell.

Brief Summary Text (16):
In accordance with one aspect of the invention the BIRA subsystem stores all information needed to allocate spare rows and columns in a set of row and column registers. Each row register corresponds available spare row, and each column register corresponds to an available column. The BIRA subsystem responds to incoming cell addresses by writing each included row address into a row register, by writing each included column address into a column register, and by writing link bits into the column registers. Each link bit links the row and column registers storing row and column addresses of a defective cell. The row and column addresses stored in these registers indicate the array rows and columns for which spare rows and columns are to be allocated.

Drawing Description Text (2):

FIG. 1 illustrates in block diagram form an application specific integrated circuit (ASIC) including an embedded random access memory (RAM) and a built-in self repair (BISR) system for testing and repairing the RAM;

Drawing Description Text (8):
FIG. 37 illustrates the built-in repair analysis (BIRA) subsystem of the BISR system of FIG. 1 in more detailed block diagram form;

Drawing Description Text (10):
FIG. 39 illustrates the BIRA subsystem of the BISR system of FIG. 39 in more detailed block diagram form; and

Detailed Description Text (2):
BISR System Architecture

Detailed Description Text (3):
FIG. 1 illustrates in block diagram form an application specific integrated circuit (ASIC) 10 including an embedded random access memory (RAM) 12, and other ASIC circuits 14. During normal ASIC operation, ASIC circuits 14 also read and write access RAM 12 and communicate with external devices via the ASIC's input/output (I/O) terminals 16. Since the data, address and control terminals 32 of RAM 12 are not directly accessible to external test equipment via the ASIC's I/O terminals 16, a built-in self-repair (BISR) system 18 in accordance with the invention is incorporated into ASIC 10 to test and repair RAM 12.

Detailed Description Text (4):
ASIC circuits 14 normally read and write access the address, control and data terminals of RAM 12 via a set of multiplexers 20-22 included in BISR subsystem 18. However when BISR system 18 is to test RAM 12, (for example on system power up) a built-in self-test (BIST) subsystem 24 of BISR subsystem 18 switches multiplexers 20-22 to connect BIST subsystem 24, rather than ASIC circuits 14, to RAM 12. During the test, BIST subsystem 24 writes data into each address of RAM 12, reads the data back out that address, and compares the data written into the address to the data read back out to determine whether they match. When the RAM's input and output data do not match, BIST subsystem 24 transmits an ERROR signal to tell a built-in repair analysis (BIRA) subsystem 26 that the current memory address is defective. BIRA subsystem 26 then acquires and processes the current RAM 12 input address to produce configuration data CONFIG that tells RAM 12 how to reconfigure itself to repair the defective cell. After testing all addresses of RAM 12 and signaling BIRA subsystem 26 to acquire all defective addresses, BIST subsystem 24 transmits a REPAIR signal to RAM 12 telling it to repair itself in accordance with the CONFIG data from BIRA subsystem 26.

Detailed Description Text (48):
Thus has been shown and described a BIRA subsystem of a BISR system 26 for allocating spare rows and columns of cells for replacing rows and columns of an array of memory cells in response to an input sequence of cell addresses, each identifying a row address (XADDR) and a column address (YADDR) of each defective cell of the cell array. The BIRA subsystem, including a row register (RA-RC) corresponding each spare row and a column register (CA,CB) corresponding to each spare column, responds to incoming cell addresses by writing their included row address into the row registers, by writing their column addresses into the column registers, and by writing link bits (LA-C) into the column registers. Each link bit links a row and a column register storing row and column addresses of a defective cell. The BIRA subsystem also writes a multiple cell bit (XM) into each row register to indicate when the row address it stores includes more than one defective cell. The row and column addresses stored in these registers indicate the array rows and columns for which spare rows and columns are to be allocated. Each row and column register also includes a "permanent" bit (XP or YP) the BIRA subsystem sets to indicate when the spare row or column allocation indicated by its

stored row or column address is permanent. The BIRA subsystem efficiently allocates spare row and columns by manipulating the addresses and data bits stored in the row and column registers as it processes the input sequence of defective cell addresses.

CLAIMS:

1. An apparatus for generating output configuration data allocating spare rows and columns of cells for replacing I rows and J columns of an array of memory cells in response to incoming cell addresses, each including a row address and a column address of a defective cell of said array, wherein I and J are integers greater than 0, and wherein said array is implemented in an integrated circuit (IC), the apparatus comprising:

I row registers implemented in said IC, each corresponding to a separate one of the spare rows, for storing a row address of an array row including at least one defective cell;

J column registers implemented in said IC, each corresponding to a separate one of the spare columns, for storing a column address of an array column including at least one defective cell, and for storing a set of I link bits, each corresponding to a separate one of said I row registers; and

control means for responding to an incoming cell address by writing its included row address into one of said row registers, by writing its included column address and a link bit into one of said column registers, said link bit corresponding to said one of said row registers.

4. The apparatus in accordance with claim 3

wherein when an incoming cell address includes a row address already stored in one of said row addresses, and a column already stored in one of said column registers, said control means responds to said column address by writing a link bit corresponding to said one of said row registers into said one of said column registers.

6. The apparatus in accordance with claim 5

wherein when each of said row address registers already stores a row address, and wherein an incoming cell address includes a row address not already stored in one of said row registers, said control means writes a permanent column assignment bit into a column address register storing a column address identified by said incoming cell address and removes row addresses from each row address register corresponding to a link bit stored in that column address register, provided the corresponding row address register in not currently storing a multiple cell bit.

8. The apparatus in accordance with claim 1

wherein when an incoming cell address includes a row address already stored in one of said row addresses, and a column address already stored in one of said column registers, said control means responds to said column address by writing a link bit corresponding to said one of said row registers into said one of said column registers.

10. The apparatus in accordance with claim 9

wherein when each of said row address registers already stores a row address, and wherein an incoming cell address includes a row address not already stored in one of said row registers, said control means writes a permanent column assignment bit into a column address register storing a column address identified by said incoming

cell address and removes row addresses from each row address register corresponding to a link bit stored in that column address register, provided the corresponding row address register in not currently storing a multiple cell bit.

15. A built-in self-repair (BISR) system for testing an array of rows and columns memory cells embedded in an integrated circuit (IC) and for reconfiguring said array to replace at least of said rows containing a defective cell with a spare row and for replacing at least one of said columns containing a defective cell with a spare column, each cell having a unique combination of row and column address, said array including I spare rows and J spare columns where I and J are integers greater than 0; the BISR system comprising:

a built-in self-test (BIST) subsystem incorporated into said IC for testing each cell of said array to determine whether it is defective and for generating as output a cell address of each defective cell of said array, each cell address including a row address of the defective cell and a column address of the defective cell; and

a built-in replacement analysis (BIRA) subsystem for receiving row and column addresses generated by said BIST subsystem, the BIRA subsystem comprising:

I row registers, each corresponding to a separate one of the spare rows, for storing a row address of an array row including at least one defective cell;

J column registers, each corresponding to a separate one of the spare columns, for storing a column address of an array column including at least one defective cell, and for storing a set of I link bits, each corresponding to a separate one of said I row registers; and

control means for responding to an incoming cell address by writing its included row address into one of said row registers, by writing its included column address and a link bit into one of said column registers, said link bit corresponding to said one of said row registers.

16. The BISR system in accordance with claim 15

wherein when an incoming cell address includes a column address already stored in one of said column registers, said control means responds to said column address by writing a link bit into said one of said column registers; and

wherein when an incoming cell address includes a row address already stored in one of said row addresses, and a column address already stored in one of said column registers, said control means responds to said column address by writing a link bit corresponding to said one of said row registers into said one of said column registers.

17. The BISR system in accordance with claim 16

wherein each of said row registers includes means for storing a multiple cell bit; and

wherein when an incoming cell address includes a row address already stored in one of said row registers, said control means writes said multiple cell bit into that row register to indicate that row address includes more than one defective cell.

18. The BISR system in accordance with claim 17

wherein each of said row registers includes means for storing a permanent row assignment bit, indicating a spare row is permanently assigned to replace an array row identified by the row address stored in said row register;

wherein each of said column registers includes means for storing a permanent column assignment bit, indicating a spare column is permanently assigned to replace an array column identified by the column address stored in said column register;

wherein when each of said row address registers already stores a row address and an incoming cell address includes a row address not already stored in one of said row registers, said control means writes a permanent column assignment bit into a column address register storing a column address identified by said incoming cell address and removes row addresses from each row address register corresponding to a link bit stored in that column address register, provided the corresponding row address register in not currently storing a multiple cell bit; and

wherein when each of said column address registers already stores a row address and an incoming cell address includes a column address not already stored in one of said column registers, said control means writes a permanent row assignment bit into a row address register storing a row address identified by said incoming cell address.

Previous Doc Next Doc Go to Doc#

US006304989B1

(12) **United States Patent**
Kraus et al.

(10) **Patent No.: US 6,304,989 B1**
(45) **Date of Patent: Oct. 16, 2001**

(54) **BUILT-IN SPARE ROW AND COLUMN REPLACEMENT ANALYSIS SYSTEM FOR EMBEDDED MEMORIES**

(75) Inventors: **Lawrence Kraus**, San Jose; **Ivan-Pierre Batinic**, San Martin, both of CA (US)

(73) Assignee: **Credence Systems Corporation**, Fremont, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **09/358,689**

(22) Filed: **Jul. 21, 1999**

(51) **Int. Cl.**[7] **G01R 31/28**
(52) **U.S. Cl.** **714/733**; 714/718
(58) **Field of Search** 395/401; 714/710, 714/711, 7, 733, 718; 365/200, 201

(56) **References Cited**

U.S. PATENT DOCUMENTS

5,577,050		11/1996	Bair et al.	714/710
5,602,999	*	2/1997	Hyatt	395/401
5,758,056	*	5/1998	Barr	714/710
5,764,878		6/1998	Kablanian et al.	714/7
5,920,515	*	7/1999	Shaik et al.	365/200
5,987,632	*	11/1999	Irrinki et al.	714/711
6,065,134	*	5/2000	Bair et al.	714/7
6,067,262	*	5/2000	Irrinki et al.	365/201
6,141,779	*	10/2000	Hill et al.	714/710

* cited by examiner

Primary Examiner—David Ton
(74) *Attorney, Agent, or Firm*—Daniel J. Bedell; Smith-Hill and Bedell

(57) **ABSTRACT**

A built-in replacement analysis (BIRA) circuit allocates spare rows and columns of cells for replacing rows and columns of an array of memory cells in response to an input sequence of cell addresses, each identifying a row address and a column address of each defective cell of the cell array. The BIRA subsystem, including a row register corresponding each spare row and a column register corresponding to each spare column, responds to incoming cell addresses by writing their included row address into the row registers, by writing their column addresses into the column registers, and by writing link bits into the column registers. Each link bit links a row and a column register by storing row and column addresses of a defective cell. The BIRA subsystem also writes a "multiple cell" bit into each row register to indicate when the row address it stores includes more than one defective cell. The row and column addresses stored in these registers indicate the array rows and columns for which spare rows and columns are to be allocated. Each row and column register also includes a "permanent" bit the BIRA subsystem sets to indicate when the spare row or column allocation indicated by its stored row or column address is permanent. The BIRA subsystem efficiently allocates spare row and columns by manipulating the data stored in the row and column registers in response to a sequence of defective cell address.

18 Claims, 11 Drawing Sheets